Final Program Overview *(Subject to updates and changes)*

	DAY 1: December 2, 2025
8:00am – 8:45am	Registration & Refreshment
8:45am	**Attendees to be seated**
Venue	Resort World West Ballroom at Basement 2
9:00am - 9:10am	Welcome Speech: Prof Eric Phua, EPTC 2025 General Chair
9:10am - 9:20am	Opening Speech: Prof Jeffery Suhling (EPS President-Elect)
9:20am - 10:05am	Keynote 1: Dr Radha Nagaranjan, SVP/CTO, Marvell **Scaling AI Infrastructure with Advanced Optical Interconnects**
10:05am - 10:30am	25min Coffee Break @ West Ballroom Foyer
10:30am - 11:15am	Keynote 2: Audrey Charles, SVP, Lam Research **Interconnect Horizons: Wafer and Panel Innovation and Industry Partnerships to Unlock AI's Next Step**
11:15am - 12:15pm	Panel Session: Advances and Challenges in Metrology and Test for Heterogeneous Integration Moderator: Pax Wang, UMC Panelist: Dr James S. Papanu (TEL), Dr Sia Choon Beng (FormFactor), Bhupi Kumar (KLA-Tencor)
12:15pm - 12:35pm	Technology Solution Presentation: by Lam Research (Diamond Sponsor)
Venue	West Ballroom Foyer
12:35pm - 1:40pm	Lunch @ West Ballroom 1 and Foyer
	Exhibition Hall Opens (LEO 1-4 Function Room at Level 1)
Venue	Resort Worlds West Ballroom at Basement 2
1:40pm - 2:25pm	Keynote 3: Pax Wang, TD Director, UMC **Rewiring Edge AI System Efficiency with Advanced Packaging**
2:25pm - 2:40pm	Technology Solution Presentation: by Applied Materials (Platinum Sponsor)
2:40pm - 3:25pm	Keynote 4: Prof. Harald Kuhn, Director, Fraunhofer Institute of Electronic Nano Systems ENAS **Driving Innovation Through Hetero-Integration: Technologies, Challenges and Future Directions**
3:25pm - 3:50pm	25min Coffee Break @ West Ballroom Foyer
3:50pm - 4:05pm	Technology Solution Presentation: by KLA-Tencor (Platinum Sponsor)
4:05pm - 5:05pm	Panel Session: Co-Packaged Optics: The Next Inflection Point for Advanced Packaging Moderator: Dr Surya Bhattacharya (IME) Panelist: Dr Torsten Wipiejewski (Huawei), Cindy Palar (Celestial AI), Dr Jagadish CV (Advanced Micro Foundry)
5:05pm - 5:45pm	Welcome Reception @ West Ballroom Foyer

DAY 2: December 3, 2025

Venue	AQUARIUS 1-2	GEMINI 1	GEMINI 2	AQUARIUS 3-4	PISCES 1	PISCES 2
	PDC1	**PDC2**	**PDC3**	**PDC4**	**PDC5**	**PDC6**
08:30am - 10:00am	Advanced Packaging for Chiplets, Heterogenous Integration and CPO **Dr John Lau (Unimicron)**	Photonic Components and Packaging Technologies for Data Center, Communications, Sensing & Displays **Dr Torsten Wipiejewski (Huawei)**	Advanced Packaging for MEMS and Sensors **Dr Horst Theuss (Infineon)**	Current and Future Challenges and Solutions in AI & HPC System and Thermal Management **Dr Gamal Refai-Ahmed (AMD)**	Overview of Characterization Techniques for 3D HI Circuit Packaging **Prof Ali Shakouri (Purdue University)**	Design-on Simulation Technology for Reliability Prediction of AP **Prof K.N. Chiang (National Tsing Hua University)**
10:00am - 10:30am	30min Coffee Break outside Exhibition Hall (LEO 1-4)					
10:30am - 12:00pm	PDC1 (con't)	PDC2 (con't)	PDC3 (con't)	PDC4 (con't)	PDC5 (con't)	PDC6 (con't)
12:00pm - 1:15pm	EPS Luncheon @ PISCES 3 to Virgo 3					
1:15pm - 2:25pm	Technology Innovation Showcase - Session 1 (70 min) | Quiz & Prizes Included					
Venue	AQUARIUS 3	AQUARIUS 4	GEMINI 1	GEMINI 2	PISCES 1	PISCES 2
2:25pm - 3:10pm	**A1. Materials and Processing 1**	**A2. TSV/Wafer Level Packaging 1**	**A3. Mechanical Simulation & Characterization 1**	**A4. Interconnection Technologies 1**	**A5. Advanced Packaging 1**	**A6. Emerging Technologies**
Session Chair	Alvin Lee, Brewer Science	Sungdong KIM, SeoulTech	Jeff Suhling, University of Auburn	Ksenija Varga, EV Group	Karsten Meier, TU Dresden	Christian Tschoban, IZM
2:25pm - 2:40pm	A1.1 (P372) **(111)-Oriented Nanotwinned/ Nanograined Bilayer Cu for Post-Q-time Low Temperature Cu-Cu Bonding** Peng, Gangqiang City University of Hong Kong, Hong Kong	A2.1 (P168) **Thermally Reliable Through Glass Via Filling with Ni-Fe Alloy for Advanced 3D Packaging (MAT)** Yang, Fan Hanyang University, Korea	A3.1 (P317) **Toward lifetime prediction under variable load conditions in power electronics** Horn, Tobias Daniel Micro Materials Center, Fraunhofer ENAS, Chemnitz, Germany	A4.1 (P266) **Surface Treatment for Wafer Bonding using Atmospheric Vapor Plasma Technology** Lee, Seokjun Samsung Electronics, Korea	A5.1 (P170) **Development of Embedded Bridge Die interposer Using FO Packaging for HI of NPUs and HBMs** Kim, Jay nepes, Korea	A.6.1 (P326) **3D Surface Ion Trap Process Development for Quantum Applications** Li, Hongyu Institute of Microelectronics, A*STAR, Singapore
2:40pm – 2:55pm	A1.2 (P167) **Enhancing Wafer Bonding Strength via Surface and Dielectric Modification Using Plasma Activation Process** Park, Jaehyung Samsung Electronics, Korea	A2.2 (P319) **RDL-first FOWLP Development for III-V Semiconductor Chips in RF Applications** Ho, Soon Wee David Institute of Microelectronics, A*STAR, Singapore	A3.2 (P255) **Board level solder reliability and package stress for TSiCV UBM/bump IC package design** Mandal, Rathin Institute of Microelectronics, A*STAR, Singapore	A4.2 (P185) **Study of Extremely Low Temperature Organic Hybrid Bonding with Grain Engineered Cu** Maruyama, Yoshiki Resonac Corporation	A5.2 (P287) **HI of High-Performance Compute, Memory and Photonic Engine Chiplets on Large Molded Interposer package** Chai, Tai Chong Institute of Microelectronics, A*STAR, Singapore	A6.2 (P161) **2.5D Cryogenic Packaging for Advanced Quantum Processors** Jaafar, Horhanani Institute of Microelectronics, A*STAR, Singapore
2:55pm – 3:10pm	PA1.3 (P356) **Analysis of SiO_2 surface chemistry by quasi-in situ XPS during N_2 plasma activation for SiO_2/SiO_2 bonding** Jin, Renxi Institute of Microelectronics of the Chinese Academy of Sciences, China	A2.3 (P302) **Mitigating Connected PAD Corrosion in Hybrid Bonding** Chew, Soon Aik IMEC, Belgium	A3.3 (P138) **Design of Wire Bonding Schemes for Reliability of CQFP Packages under Vibration Test** Ma, Yiyi STMicroelectronics, Singapore	A4.3 (P355) **Bond line thickness stability of Cu sintering for automotive power module packaging** Kim, Byeongchan Korea Institute of Industrial Technology, Korea	A5.3 (P199) **Ultra-low-TTV Glass Carrier and Temporary Bonding Method to Enable Wafer Ultra-thinning** Chang, Ya Huei Corning incorporated	A6.3 (P208) **Wafer-level Processes for the Manufacturing of Encapsulated Flexible Polymer-Based Implants** Costina, Andrei Fraunhofer IZM

DAY 2: December 3, 2025 (con't)

3:10pm - 4:40pm	Interactive Presentation 1 (Poster), Exhibition and Coffee Break outside Exhibition Hall (LEO 1-4)					
Venue	AQUARIUS 3	AQUARIUS 4	GEMINI 1	GEMINI 2	PISCES 1	PISCES 2
4:40pm -5:40pm	**B1. Materials and Processing 2**	**B2. Thermal Management and Characterization 1**	**B3. Mechanical Simulation & Characterization 2**	**B4. Interconnection Technologies 2**	**B5. Advanced Packaging 2**	**B6. Assembly and Manufacturing Technology 1**
Session Chair	Kim Shyong Siow, UKM	Kazuyoshi FUSHINOBU, Tokyo Institute of Technology	Seungbae Park, Binghamton University	James Papanu, TEL	RHEE Minwoo, SAMSUNG	Haruichi Kanaya, Kyushu University
4:40pm – 4:55pm	B1.1 (P343) **Chip Stacking: Impact of Chip Spacing in C2W hybrid bonding on Temporary Bonding and Debonding** Sharma, Jaibir Institute of Microelectronics, A*STAR, Singapore	B2.1 (P251) **DIMM Thermal Performance Enhancement with Heat Spreader and Advanced Cooling Solutions** Nallavelli, Ramesh Micron Technology Operations India LLP	B3.1 (P332) **Prediction of Void-induced Crack Propagation within Underfill using the Meshless Material Point Method** de Jong, Sjoerd Douwe Medard Delft University of Technology	B4.1 (P188) **A Novel Interface Characterization Technique for Hybrid Bonding Process Optimization** Sameshima, Junichiro Toray Research Center, Inc., Japan	B5.1 (P354) **Innovation and Efficiency in 3D Packaging Enabled by Optimized Integration Processes** Varga, Ksenija EV Group, Austria	B6.1 (P201) **High-Density Interconnect RDL-FPC Hybrid Substrate for Compact SiP Packaging** Li, Jeng-Ting Unimicron Technology Corp., Taiwan
4:55pm – 5:10pm	B1.2 (P382) **Water Vapor Permeation in Low-Temperature Processable Polyimide Materials for Reliable Polymer HB** Nomura, Kota Toray Industries Inc., Japan	B2.2 (P223) **CFD and Surrogate Model-Driven Optimization of Two-Phase Immersion Cooling Configurations** Jalali, Ramin National Yang Ming Chiao Tung University	B3.2 (P271) **Enhancing Predictive Accuracy of Warpage and Reliability for Advanced Packages by Modelling Accurate Poisson's Ratio in FEM** Che, Faxing Micron Semiconductor Asia Operations Pte. Ltd	B4.2 (P174) **Gas-Free & Nano TiO2-Coated Ag Bonding Wire for Replacing Au Wire** Park, Soojae OxWires Co., Ltd., Korea	B5.2 (P275) **Seamless Heterointegration of Components: Advancements in Fanout Technology and Thermal Solutions in SIP** Gernhardt, Robert Fraunhofer IZM, Germany	B6.2 (P365) **Novel UV-USP Laser Grooving and Plasma Dicing Separation Schemes for Next Generation Advanced Packaging** Evertsen, Rogier ASMPT ALSI, The Netherlands
5:10pm – 5:25pm		B2.3 (P153) **Thermal Design and Power Dissipation of Advanced Package with Heterogenous Integration** Han, Yong Institute of Microelectronics, A*STAR, Singapore	B3.3 (P294) **Optimization of Warpage and Mechanical Properties for Stacked SIP Package** Liu, Zhen Changsha AnMuQuan Intelligent Technology Co., Ltd, China	B4.3 (P280) **High-AR, Fine-Pitch Through-Mold Interconnect Fabrication for Heterogeneous Integration of HPC** Chia, Lai Yee Institute of Microelectronics, A*STAR, Singapore	B5.3 (P102) **A Packaging Structure for an Antenna-in-Package Module** Tain, Ra-Min Unimicron Technology Corporation, Taiwan	B6.3 (P173) Is **Flash Lamp Annealing a Relevant Wafer Debonding Technique?** Jedidi, Nader IMEC, Belgium
5:25pm – 5:40pm	B1.4 (P362) **Applicability of Both-Sided Flash Lamp Annealing (FLA) Method on Heat Treatment Cu Plating Thin Film and Low Dielectric Resin Films** Yi, Dong Jae Graduate School of Engineering, Kanto Gakuin University	B2.4 (P142) **PIV-Based Study of Heat Dissipation and Clogging phenomenon of TiO_2 Nanofluid in Microchannels** Li, Tieliang Xidian University, China	B3.4 (P239) **Thermal and mechanical properties optimization of TGV interposer for 2.5D integrated transceiver** Li, Chunlei Xiamen University; Sanming University, China	B4.4 (P144) **Interfacial Reactions of BiIn and SnBi Solders React with Cu Substrate** Wang, Yi-Wun Tamkang University, Taiwan	B5.4 (P303) **Using WGAN-Based Data Augmentation Machine Learning Algorithm for Estimating the Equivalent Material Properties** Su, Qinghua National Tsing Hua University, Taiwan	B6.4 (P301) **Cost efficient Infrared Laser debonding technology enabled by Si carrier reuse** Chancerel, Francois IMEC, Belgium
5:40pm - 6:45pm	Sponsors/Exhibitors Appreciation and Networking Cocktail Session @ AQUARIUS 1 & 2					

DAY 3: December 4, 2025

Venue	AQUARIUS 3	AQUARIUS 4	GEMINI 1	GEMINI 2	PISCES 1	PISCES 2
8:45am -10:45am	**C1. TSV/ Wafer Level Packaging 2**	**C2. Smart Manufacturing and Equipment Technology 1**	**C3. Mechanical Simulation & Characterization 3**	**C4. Quality, Reliability & Failure Analysis 1**	**C5. Advanced Packaging 3**	**C6. Assembly and Manufacturing Technology 2**
Session Chair	Peng Zhao, imec	Sachin Dangayach, AMAT	Chiang Kuo Ning, National Tsing Hua University	Xue Ming, Infineon	Toh Chin-Hock, Lam Research	Dongshun Bai, Brewer Science
8:45am – 9:00am	C1.1 (P106) **Adaptive Patterning®: Unlocking Scalable Density in Embedded Bridge Die Interposer** Sandstrom, Clifford Paul Deca Technologies, United States of America	C2.1 (P242) **Connectivity-Guided Feasibility Masking for Efficient Chiplet Placement in 2.5D Packaging via Reinforcement Learning** Kundu, Partha Pratim Institute for Infocomm Research (I2R), A*STAR, Singapore	C3.1 (P177) **Study on the Warpage Simulation and its Validation of Lidded FCBGA with Indium alloy TIM** Park, Yoonsoo Amkor technology, Inc., Korea	C4.1 (P140) **Studies and Elimination of F-induced Corrosion on Al Bondpads and Wafer Fabrication Process Improvement** Hua, Younan WinTech Nano-Technology Services Pte. Ltd., Singapore	C5.1 (P312) **Characterization of PVD Seed Layer Contact Resistance in 2.0 to 20.0 µm Vias** Carazzetti, Patrik Evatec AG, Switzerland	C6.1 (P273) **Selective Post-Soldering Volume Adjustment for Improved Co-Planarity of C4 Bump** Fettke, Matthias PacTech GmbH, Germany
9:00am – 9:15am	C1.2 (P336) **Novel Selective Copper Deposition Method for TGV Filling** Seo, Jong Hyun Cuprum Materials Inc., Korea	C2.2 (P263) **Real-Time 3D Reconstruction for Wire Bonding Using Multi-View Projection and EM Polynomial Modelling** Chien, Yu Hsuan ASMPT, Taiwan	C3.2 (P233) **A Shock Vibration Calculation Method Considering Viscoplastic Behavior of Packaging Systems** Chen, Honghao Nanjing University of Posts and Telecommunications	C4.2 (P374) **WireBond Challenges of Copper Clip for Multi-Die Controller MOSFET Package** Chantana Tangcharoensuk NXP Manufacturing, Thailand	**C5.2 (P150) 112 Gbps SERDES Channel Design with 2.5D Sub-Micron BEOL Interconnect** Ayers, Seann Applied Materials, United States of America	C6.2 (P178) **Aerosol Jet Printing of a Copper Nanoparticle Ink by Controlling the Wetness of Aerosols** Zheng, Cheng Nanyang Technological University, Singapore
9:15am – 9:30am	C1.3 (P172) **Thin Fan-Out Package Characterization and Evaluation** Lin, Vito Siliconware Precision Industries Co., Ltd., Taiwan	C2.3 (P186) **Defect Localization in Material Surfaces Using retinal CSRF kernel and Statistical Peak Profiling** Hanmante, Udaykumar Applied Materials	C3.3 (P113) **Delamination Effect Investigations Near RDL and UBM in WLCSP Packages** Huang, Leo Renesas, Taiwan	C4.3 (P306) **Direct Bonding of Aluminum and Polypropylene in High-Reliability Structural Interfaces** Park, Jin Woong Hanbat National University, Korea	C5.3 (P151) **Advanced Bevel Deposition for Enhanced Yield and Cost Efficiency in Wafer-Level Bonding** Xiao, Yun Lam Research, China	C6.3 (P162) **Heat Release Tape Characterization for Panel Level Packaging** Shanmuga Sundaram, Shanthini ST Microelectronics, Singapore
9:30am – 9:45am	C1.4 (P111) **Process-induced parasitic surface conduction (PSC) in SOI substrates for 3D-integrated RF front-end applications** Rotaru, Mihai Dragos Institute of Microelectronics ASTAR, Singapore	C2.4 (P187) **Enhancing Wire Bonding Quality Prediction with a Physics-Informed Ensemble Learning Framework** Lu, Hsin-Fang ASMPT Limited, Taiwan	C3.4 (P368) **Feasibility Study of Stacked Sub-THz Band AiP Modules Based on Warpage and Stress Analysis** Tsukahara, Makoto SHINKO ELECTRIC INDUSTRIES CO., LTD., Japan	C4.4 (P219) **Nanoindentation tests and constitutive study of sintered nano-silver** Yu, Huachen Nanjing University of Posts and Telecommunications, China	C5.4 (P307) **Physics-Informed Graph Convolutional Neural Network for Scalable, and Accurate Thermal Analysis of 2.5D Chiplet-based Systems** Sahay, Rahul Singapore University of Technology and Design, Singapore	C6.4 (P175) **Reliability Evaluations of Pb-free Solder Joint Formed Using Sn-Ag-Cu solder ball and Sn-Bi-Ag solder paste** Kim, Jahyeon Korea Institute of Industrial Technology (KITECH), Hanyang University, Korea
9:45am -10:15am	30min Coffee Break outside Exhibition Hall (LEO 1-4)					
10:15am -10:45am	**Invited Talk 1:** **Dr Dielacher Bernd** (EVG) The Critical Role of Wafer Bonding in Next-Generation Interconnect Scaling	**Invited Talk 2:** **Taichi Suzuki** (ULVAC Inc) Polymer Fine Pattern Formation based upon Plasma Etching for High Density RDL Interposer	**Invited Talk 3:** **Dr Zhao Yi** (ZSCT) Advanced Packaging EDA's New Paradigm: Collaborative Innovation Revolution for Design-Simulation-Verification in the 2.5D/3D Era	**Invited Talk 4:** **Inohara Masahiro** (KIOXIA) Accelerating the Evolution of NAND Flash Memory with Bonding Technologies	**Invited Talk 5:** **Dr Mushuan Chan** (SPIL) High Layer RDL Process Technology for Heterogenous Integration Package	**Invited Talk 6:** **Dr Sajay BG** (IME) Heterogeneously Integrated WL Processed CPO Engine for Next Gen AI/ML Data Centers
Venue	PISCES 3 to VIRGO 3					
10:45am - 11:55am	Technology Innovation Showcase Session 2 (70 min) | Quiz & Prizes Included					
Venue	PISCES 3 to VIRGO 3					
11:55am -1:00pm	EPTC Luncheon @ PISCES 3 to VIRGO 3					

DAY 3: December 4, 2025 (con't)

11:55am -1:00pm	EPTC Luncheon @ PISCES 3 to VIRGO 3					
Venue	AQUARIUS 3	AQUARIUS 4	GEMINI 1	GEMINI 2	PISCES 1	PISCES 2
1:00pm -1:45pm	**D1. Materials and Processing 3**	**D2. Thermal Management and Characterization 3**	**D3. Mechanical Simulation & Characterization 4**	**D4. Interconnection Technologies 3**	**D5. Advanced Packaging 4**	**D6. Quality, Reliability & Failure Analysis 2**
Session Chair	Lan Peng, imec	Gamal Refai-Ahmed, AMD	Faxing Che, Micron	Torsten Wipiejewski, Huawei	Albert Lan, AMAT	Tain RaMin, Unimicron
1:00pm – 1:15pm	D1.1 (P164) **Metallurgical properties of Sn-3.0Ag-0.5Cu solder joints with Alumina layer deposition** Noh, Eun-Chae Chungbuk National University, Korea	D2.1 (P191) **Magnetohydrodynamic Liquid Cooling Embedded in PCBs for High-power Electronics** Feng, Huicheng A*STAR, Singapore	D3.1 (P252) **Evaluating Dummy Die Sizes and Compound Adjustments to reduce Wafer Warpage in FOEB-T Packaging.** Zeng, TzuChi Siliconware Precision Industries Co., Ltd., Taiwan	D4.1 (P202) **Comparative wear-out study and characterization methods for Pure and Alloyed Copper wires** Losacco, Gabriele STMicroelectronics, Italy	D5.1 (P320) **Ka-Band Ultra-Short Die-to-Antenna Interconnect Enabled by Embedded Glass Fan-Out Packaging** Jin, Shengxiang Peking University Shenzhen Graduate School, China	D6.1 (P141) **Short-Circuit Behavior and Failure Mechanism Analysis of Double-Trench SiC MOSFETs** Chen, Zhiwen The Institute of Technological Sciences, Wuhan University, Wuhan, China
1:15pm – 1:30pm	D1.2 (P211) **Wettability, Mechanical Properties and IMC of SiC nanoparticle-reinforced Sn-58Bi solders on Cu substrates under multiple reflow cycles** Yao, Wang Harbin Institute of Technology	D2.2 (P270) **Numerical Investigation of Embedded Micro-Pin Fin Two-Phase Liquid Cooling for Dual-Chip Stacks in HPC & AI Applications** Patra, Chinmaya Kumar Indian Institute of Technology Kharagpur, India	D3.2 (P369) **Characterization and Modelling of Inelastic Behavior of Epoxy Molding Compounds** Tippabhotla, Sasi Kumar Institute of Microelectronics, A*STAR, Singapore	D4.2 (P378) **MDQFN™: Panel-Level QFN for Scalable, Cost-Effective Semiconductor Packaging** Castillo, Chelo Veronica Deca Technologies, Inc., United States of America	D5.2 (P227) **Development of a Wideband Energy Harvesting Circuit Utilizing Terrestrial Digital Broadcast Signals** Tanaka, Hayato Kyushu University, Japan	D6.2 (P276) **A Modified Test Vehicle Incorporating DNP-Induced Strain Gradients for Single-Specimen Fatigue Life Assessment of Solder Joints** Park, Hyeong-Bin Hanyang University, Korea
1:30pm – 1:45pm	D1.3 (P304) **Impact of Solder Powder Size on Cleaning Efficiency in Chip Resistor Assemblies for Future Advanced Packaging** Parthasarathy, Ravi ZESTRON Americas, United States of America	D2.3 (P228) **Annealing effect for Backside Metallization of SiC device** Dr. Junichiro Sameshima Toray Research Center, Inc., JP	D3.3 (P220) **Nanoindentation Test and Crystal Plasticity Finite Element Model of SAC305 Solder Joint Considering Crystal Orientation** Liu, Lu Nanjing University of Posts and Telecommunications, Nanjing, China	D4.3 (P157) **Investigation of Cu bonding wire lifetime under accelerated temperature environments** Azuma, Shinya Nippon Micrometal Corporation, Japan	D5.3 (P146) **Optimization of Shielded Capacitive Power Transfer (S-CPT) Systems Using Slotted Electrodes** Chen, Hao Kyushu University, Japan	D6.3 (P147) **Correlation Between Thermal Cycling Ramp Rates and its Respective Solder Joint Reliability** CHAN, Yong Tat STMicroelectronics Pte Ltd, Singapore
1:45pm - 3:15pm	Interactive Presentation 2 (Poster), Exhibition and Coffee Break outside Exhibition Hall (LEO 1-4)					

DAY 3: December 4, 2025 (con't)

Venue	AQUARIUS 3	AQUARIUS 4	GEMINI 1	GEMINI 2	PISCES 1	PISCES 2
3:15pm -4:00pm	**E1. Materials and Processing 4**	**E2. Thermal Management and Characterization 4**	**E3. Mechanical Simulation & Characterization 5**	**E4. Interconnection Technologies 4**	**E5. Advanced Packaging 5**	**E6. Assembly and Manufacturing Technology 3**
Session Chair	Jie Wu, Henkel	L. Winston Zhang, University of Illinois at Urbana-Champaign	Chai Tai Chong, IME	Po-Hao Tsai, Applied Materials	Chuan Seng Tan, NTU	Cheng Yang, JCET
3:15pm – 3:30pm	E1.1 (P379) **Enhancing Yield Performance in Chip-to-Wafer Hybrid Bonding in Advanced Packaging** Xie, Ling Institute of Microelectronics, A*STAR, Singapore	E2.1 (P371) **Direct-Bonded Manifold-Jet- Impingement Cooling for High-Performance AI Chips** Zhang, Yuantong Xi'an Jiaotong University, China	E3.1 (P352) **Statistical Evaluation of Bond Strength Variation in Hybrid Bonding Interfaces** Kobayashi, Daiki YOKOHAMA National University, Japan	E4.1 (P299) **Fluxless Die to Die Bonding of 10µm Ultra-fine Pitch Microbump** Xu, Zheqi Tsinghua University, China	E5.1 (P367) **Low Temperature Post Bond Anneal for Hybrid Bonding enabled by Interfacial (IF) Metal Capping – An Assessment of Reliability** Rath, Santosh Kumar Applied Materials Singapore, Singapore	E6.1 (P196) **Growth Behaviour of Intermetallic Compounds in Cu-Sn3.5Ag Solder Joints with Different furnace cooling rate** Gan, Jingjian NXP Semiconductors, China
3:30pn – 3:45pm	E1.2 (P234) **Study on Backside Metallization for the S-SWIFT(TM) Package** Jo, Dambi Product Development Team, Amkor Technology, Korea	E2.2 (P334) **High-Temperature Pressure Mapping of TIM Interfaces for Improved Thermal Simulation Accuracy** U, Srinath Cisco Systems (India) Private Limited, Bengaluru, India	E3.2 (P349) **Real-time Effective Mechanical Property Characterization of Redistribution Layer (RDL) for Chiplet Integration** Liu, Jun Institute of High-Performance Computing, A*STAR, Singapore	**E**4.2 (P314) **Novel Ultrasonic Flip Chip Bonding Approach utilizing electroplated Aluminium pillars for Advanced Packaging** Cirulis, Imants Technical University Chemnitz, Fraunhofer ENAS, Germany	E5.2 (P323) **Backside Metal Interconnect for High Performance RF Interposer** Lim, Teck Guan Institute of Microelectronics, A*STAR, Singapore	E6.2 (P158) **Hybrid Evaluation of Pure Argon Plasma Treatment for Enhanced Wire Bonding and Manufacturing Efficiency in Microelectronics** Pelingo, Jorell onsemi Carmona, Philippines
3:45pm – 4:00pm	E1.3 (P189) **Study of Coverage Decay Mechanism of Liquid Metal Filler TIM for Advanced Package Application** Jhan, Jyun-De Siliconware Precision Industries Co., Ltd., Taiwan	E2.3 (P222) **Operando Thermal Analysis of CPU and PCB using a Pixel-level Emissivity Correction Method** Kim, Seongjin Pohang University of Science and Technology (POSTECH), Korea	E3.3 (P274) **Simulation and Validation of Warpage in Ultrathin Embedded-Die Substrates for Advanced Packaging** Ma, Rui Institute of Microelectronics of the Chinese Academy of Sciences, China	E4.3 (P353) **Interfacial Electromigration Behavior and Reliability Evaluation in Cu/Ag Sintered Joints** Kim, Yun-Chan Korea Institute of Industrial Technology, Korea University, Korea	E5.3 (P256) **Surface Activation and Bonding Mechanisms of SiCN and TEOS Dielectrics for Low-Temperature Hybrid Bonding** Chang, Liu School of Integrated Circuits, Southeast University, China	E6.3 (P363) **Comparative Evaluation of FCVA and High-Current Arc Deposited ta-C Films for Hermetic Encapsulation (Mat Paper)** Li, Ying Nanyang Technological University, Singapore

EPTC Luncheon @ PISCES 3 to VIRGO 3

Venue	PISCES 3 to VIRGO 3					
4:00pm - 5:10pm	Technology Innovation Showcase Session 3 (70 min) | Quiz & Prizes Included					
Venue	AQUARIUS 3	AQUARIUS 4	GEMINI 1	GEMINI 2	PISCES 1	PISCES 2
5:10pm - 5:55pm	**F1. Materials and Processing 5**	**F2. Thermal Management and Characterization 5**	**F3. Quality, Reliability & Failure Analysis 3**	**F4. Interconnection Technologies 5**	**F5. TSV/ Wafer Level Packaging 3**	**F6. Assembly and Manufacturing Technology 4**
Session Chair	Yu Shoji, Toray Industries Inc	Ali Shakouri, Purdue University	Fu Chao, WinTech Nano	Lois Liao, WinTech Nano	Soon Aik Chew, imec	Mandal Rathin, IME
5:10pm – 5:25pm	F1.1 (P116) **Study on Microstructural Evolution Mechanisms of Amorphous SiO2 in Through Glass Via Wafer during Thinning** Xu, Kezhong Huazhong University of Science and Technology, China	F2.1 (P163) **Thermal Performance Enhancement of Stacked Packages using Silicon-Based Heat Spreading Die** Lee, Seokjun Daniel Semiconductor R&D Center, Samsung Electronics, Korea	F3.1 (P115) **Defect Z-depth Determination in 2.5D IC Using Magnetic Field Imaging** Cai, Fengkai National University of Singapore, Singapore	F4.1 (P261) **Microstructure Evaluation of Engineered Cu for Low-Temperature Cu-Cu Hybrid Bonding** Tanaka, Fabiana Lie Yokohama National University, Japan	F5.1 (P105) **Analysis of Cu and dielectric layer interfacial delamination in chip redistribution layer** Chen, Zhiwen Wuhan University, China	F6.1 (P315) **Automated In-Line Metrology of Advanced Package Interconnections using a High-Speed 3D X-ray System** Gregorich, Thomas Zeiss SMT, United States of America
5:25pm – 5:40pm	F1.2 (P272) **Optimizing SSD Performance with One-Part Thermal Gap Fillers: A Sustainable Approach** Kumaresan, Vigneshwarram SanDisk Storage Malaysia, Malaysia	F2.2 (P381) **Solid-State On-Chip Thermal Management Using Micro-Thermoelectric Devices** Kim, Jeong-Hwan Korea Advanced Institute of Science and Technology, Korea	F3.2 (P200) **In-Situ Package Level Relative Humidity Measurement using Wet-Bulb and Dry-Bulb Temperatures** Iyer, Vidya Subramanian Infineon Technologies Asia Pacific; Nanyang Technological University, Singapore	F4.2 (P179) **A Molecular Dynamics Study of Grain Size Effects on Cu-Cu Interfacial Void Reduction in Direct Bonding Interconnect** Park, Junhyeok Ulsan National Institute of Science and Technology, Korea	F5.2 (P126) **Mitigation of Cu Nodule Formation in High Open Area Products for Electroplated Cu RDL Applications** Lin, SW Lam Research Corporation, Taiwan	F6.2 (P224) **Mass Transfer solution for Micro-LEDs based displays** Raphoz, Natacha CEA - LETI, France
5:40pm 5:55pm	F1.3 (P316) **Cost-Effective Wafer Level Micro Bumping Solution for Advanced Packaging** Lip Huei, Yam Heraeus Materials Singapore Pte Ltd, Singapore	F2.3 (P322) **Thermal Sensitivity Analysis of SoIC Face-to-Back Stacking Using Foundation Models for Physics** Kabaria, Hardik Vinci4D.ai Inc, USA	F3.3 (P358) **AI-empowered 3D X-ray analysis of solder joint cracking after board level vibration testing** Ghorbani, Amir Tu Delft, Netherlands	F4.3 (P243) **In-situ AFM Analysis of Thermal Expansion of Cu Pads with Varied Grain Characteristics** Yang, Gangli School of Integrated Circuits, Southeast University, China	F5.3 (P265) **Characterization on Fan-Out Heterogeneous Integration Packaging for Premium Smartphone** Chen, Cheng Chia Siliconware Precision Industries Co., Ltd., Taiwan	F6.3 (P118) **Enhancing Electrochemical Migration Resistance of Sintered Silver by Ceria Additives for Die Attachment Applications** Siow, Kim Shyong Universiti Kebangsaan Malaysia
06:15pm - 08:30pm	Party @ Ola Beach (ticketed event)					

DAY 4: December 5, 2025

Venue	VIRGO 1-3					GEMINI 2
8:45am – 10:00am	Technology Innovation Showcase Session 4 (75 min) | Quiz & Prizes Included					R10 EPS Chapter Officers' Meeting
10:00am - 11:00am	60min Coffee Break outside Exhibition Hall (LEO 1-4)					
Venue	PISCES 1	PISCES 2	PISCES 3	PISCES 4	GEMINI 1	GEMINI 2
Session Chair	Toh Chin-Hock, Lam Research	Rajoo, Ranjan, Globalfoundries	David Gani, STMicroelectronics	ZHANG Xiaowu, IME	Hua Younan, WinTech Nano	Luan Jing-En, STMicroelectronics
11:00am -11:30am	**Invited Talk 7:** **Dr Kathy Yan** (TSMC) From Cloud AI to Edge AI: Driving Innovation with Advanced Packaging	**Invited Talk 8:** **Dr Takenori Fujiwara** (Toray) Polymer Bonding Technology for Semiconductor Advanced Packaging	**Invited Talk 9:** **Dr Tan Yik Yee** (Yole Group) AI Is Accelerating the Shift to Advanced Packaging with FOPLP	**Invited Talk 10:** **Jonathan Abdilla** (BESI) Hybrid Bonding and Fluxless TCB: Defining the Sub 10um Interconnect Roadmap for 3D HI	**Invited Talk 11:** **Dr Fu Chao** (WinTechNano) Lableless Enable Effective FA of Electronics Packages through Scientific Approach	**Invited Talk 12:** **Prof Ali Shakouri** (Purdue University) Thermal Characterization and AI Analytics for 3D Heterogeneous Integrated Circuits
11:30am – 12:15pm	**G1. Advanced Packaging 6**	**G2. Materials and Processing 6**	**G3. Smart Manufacturing and Equipment Technology 2**	**G4. Interconnection Technologies 6**	**G5. Quality, Reliability & Failure Analysis 4**	**G6. Mechanical Simulation & Characterization 6**
11:30am -11::45pm	G1.1 (P350) **Fabrication of N77/N79 Antenna-plexer: Integration of BAW Filters with Broadband Glass-IPD Diplexer for 5G Applications** Park, Minsoo Korea Electronics Technology Institute, Korea	G2.1 (P240) **Copper Pillar Bump FCBGA Underfill Process Characterization for Automotive Application** Koey Poh Meng, Dominic NXP Semiconductors, Malaysia	G3.1 (P193) **AI-driven Pixel-Level Defect Localization using Magnetic Current Images** Aung, Aye Phyu Phyu Institute for Infocomm Research (I2R), A*STAR, Singapore	G4.1 (P143) **UV-Assisted Fluxless Thermal-Compression Bonding Under Ambient Conditions** Kim, You-Gwon Hanyang University, Korea	G5.1 (P132) **Anomalyspy: A Generative Defect Localization in Semiconductor Packages, with X-ray Microscopy** I Made, Riko Institute of Materials Research and Engineering (IMRE), Singapore	G6.1 (P321) **Degradation Mechanism of Frequency Stability in MEMS Resonant Accelerometers** Bie, Xiaorui Institute of CAS, China
11:45am -12::00pm	G1.2 (P308) **Power and Performance Comparison between FPGA-Optics Integrated 3D SiP and equivalent board level test hardware** Pamidighantam, V Ramana LightSpeed Photonics Private Limited, Singapore	G2.2 (P212) **Enhanced Reliability of Large BGA Assemblies for AI Server and HPC Application** Wang, Huaguang Indium Corporation, United States of America	G3.2 (P236) **Research on Intelligent Prediction of 3D-IC Packaging Injection Molding Based on Machine Learning** Wu, Jie Nanjing University of Posts and Telecommunications, China	G4.2 (P244) **Characterization of Fine Line Width/Spacing RF Interconnects for Co-Packaged Optics with High I/O Density** Wu, Jia Qi Institute of Microelectronics, A*STAR, Singapore	G5.2 (P180) **Cu/SiCN wafer-to-wafer hybrid bonding interface reliability down to 400 nm pitch** Zhang Boyao imec, Belgium	G6.2 (P370) **Dev of a Reproducible, Stable, and Scalable Eval Routine for Lifetime Assessment of Power and Microelectronic Devices** Albrecht, Jan Fraunhofer ENAS; Germany
12:00pm- 12:15pm	G1.3 (P361) **Process Developments of Chip-to-Wafer assembly with HPC and Photonics Chiplets on large RDL-first interposer** Lim, Sharon Pei Siang Institute of Microelectronics, A*STAR, Singapore	G2.3 (P384) **Development and Monitoring of Gold Electroplating Process on 300mm Wafer Level** Tran, Van Nhat Anh Institute of Microelectronics, A*STAR, Singapore	G3.3 (P359) **Cross-Domain Adaptation of Automated 3D X-ray Defect Detection from HBM to Optical Transceivers** Wang, Jie Institute for Infocomm Research (I2R), A*STAR, Singapore	G4.3 (P117) **Study on Solder Core Ball Using Sn-Bi Plating for Low-Temperature Bonding** Kim, Hui Joong MKE, Korea	G5.3 (P375) **Investigations on the Mutual Effects of Electromigration and Thermal Fatigue failures of TSV Interconnects** Cheng Tian Zhangjiang Lab, China	G6.3 (P329) **Advancing Electronic Package Reliability Analysis by Predicting Solder Joint Strain Patterns Using Neural Networks** Meier, Karsten Technische Universität Dresden, Germany
Venue	VIRGO 1-3					
12:15pm -1:30pm	Conference Lunch					

DAY 4: December 5, 2025 (con't)

12:15pm -1:30pm	Conference Lunch @ VIRGO 1 to 3					
Venue	PISCES 1	PISCES 2	PISCES 3	PISCES 4	GEMINI 1	GEMINI 2
1:30pm - 2:45pm	**H1. Advanced Packaging 7**	**H2. Materials and Processing 7**	**H3. Smart Manufacturing and Equipment Technology 3**	**H4. Electrical Simulations & AI-Powered Manufacturing**	**H5. Advanced Optoelectronics and Displays**	**H6. Mechanical Simulation & Characterization 7**
Session Chair	Shaw Fong WONG, Intel	Kathy Yan, TSMC	Lee Chee Ping, Lam Research	Aoyagi Masahiro, AIST	Sajay BG, IME	Gao Jiaying, Huawei
1:30pm - 1:45pm	H1.1 (P260) **Design and Fabrication of TGV-Integrated Passive Devices on a Glass Substrate** Yi, Sang-Ho Korea Electronics Technology Institute, Korea	H2.1 (P217) **Investigation on crack propagation mechanism of Al2O3 direct bond copper substrate** Yu Shan Huang ASE	H3.1 (P348) **Inferring Wire Length and Depth from Magnetic Field Images via Deep-Spatial Physics Informed Model** Jayavelu, Senthilnath Institute for Infocomm Research (I2R), A*STAR, Singapore	H4.1 (P169) **Characteristics in the quasi-millimeter wave band of planar transmission lines formed on flexible substrates** Kimigawa, Ryoma Kyushu University	H5.1 (P267) **Assembly of optical micro-ring resonator-based ultrasound sensor for photoacoustic imaging** Lepukhov, Evgenii Tampere university, Finland	H6.1 (P139) **Key Insights into Design for Reliability of 3D NAND Packages in Solid-State Drive** Pan, Ling Micron Semiconductor Asia Pte Ltd, Singapore
1:45pm - 2:00pm	H1.2 (P154) **Residue Free TaN Etch Method for MIM Capacitor in Advanced Packaging** Zhou, Hexin Lam Research, China	H2.2 (P129) **Pressure Sintering Mechanism of Ag Nanoparticles Based on The Master Sintering Curve and Visualization of Sinterability** Hiratsuka, Daisuke TOSHIBA Corporation	H3.2 (P213) **Device-to-Package Electrothermal Performance Prediction of Power MOSFETs via Coupled Iterative Dual-Artificial Neural Networks** Dai, Yuxuan Nanjing University of Posts and Telecommunications, China	H4.2 (P289) **Development of PDK Library for Accurate Modelling of 2.5D Interconnect Structures in Heterogeneous Integration** Mani, Raju Institute of Microelectronics, A*STAR, Singapore	H5.2 (P104) **High Coupling Efficiency Adhesive for Photonic Packaging** Lim, See Chian Garian DELO Industrial Adhesives	H6.2 (P373) **A novel wafer warpage numerical model considering further shrinkage of epoxy molding compound** Ji, Lin Institute of Microelectronics, A*STAR, Singapore
2:00pm – 2:15pm	H1.3 (P221) **High-Performance Graphene Coatings for Superior Thermal and Mechanical Properties in Electronic Packaging Enclosures** Sundararajan, Muralidharan SanDisk Storage Sdh Bhd, Malaysia	H2.3 (P165) **Novel TIM1 paste for Enhanced Thermal Management** Liao, Yile Heraeus Materials Pte Ltd, Singapore	H3.3 (P209) **Thermal- and Wirelength-Aware Chiplet Placement in 2.5D Systems Through Multi-Agent Reinforcement Learning** Hou, Yubo Institute for Infocomm Research (I²R), A*STAR, Singapore	H4.3 (P264) **Generative AI-Powered Defect Detection for 3D X-ray Microscopy Scans of High Bandwidth Memory Bumps** Chang, Richard Institute for Infocomm Research (I2R), A*STAR, Singapore	H5.3 (P253) **2.5D PIC Photonic Interposer Engine for Next Generation Photonic Link CPO of High-Performance Computing and Data Communications** Chi, Ting Ta Institute of Microelectronics, A*STAR, Singapore	H6.3 (P127) **Development of Warpage Predictive Models using Physics-Driven Simulation** Yu, Wei Micron Semiconductor Asia Operations, Singapore
2:15 – 2:30pm	**Invited Talk 13** **David Gani (STMicro)** Challenges and Advantages in Panel Level Packaging	H2.4 (P232) **A novel mitigate solder short circuit in double-sided copper-exposed power modules** Yu Hsien Chien ASE	**Invited Talk 15:** **Dr Min Woo Rhee (Samsung)** Understanding of Hybrid Bonding Mechanism by Utilizing Molecular Dynamics Approach	**Invited Talk 14** **Hidenori Abe (Resonac)** Advanced Packaging Materials Innovation through Co-Creative Activities and Trends in Advanced Packaging Processes		
2:30pm - 2:45pm						
245pm – 3:05pm	20min Coffee Break outside Exhibition Hall (LEO 1-4)					

	DAY 4: December 5, 2025 (con't)
2:45pm – 3:05pm	20min Coffee Break outside Exhibition Hall (LEO 1-4)
Venue	VIRGO 1,2 and 3 (combined rooms)
3:05pm - 5:05pm	**Heterogeneous Integration Roadmap (HIR) Workshop** Theme: Interconnects - Design and Manufacturing of Complex HI Structures Opening: Kitty Pearsall Design for Manufacturability of > 1 kW: Gamal Refai Ahmed (AMD) Photonics Design: Amr S Helmy (University of Toronto) HBI Manufacturability HBI: Loke Yuan Wong (Applied Materials) TCB Manufacturability: Li Ming (ASMPT) CPO Manufacturability: Surya Bhattacharya (IME, A*STAR) Panel Discussion "Why HBI/CPO HVM Adaption is in Slower Pace Despite all the Buzz?" Moderator: Wong Shaw Fong (Intel)
5:10pm - 5:30pm	Closing Ceremony and Lucky Draw @ VIRGO 1, 2 and 3 (combined rooms)